What is claimed is:

1. A configurable mirror sense amplifier system for flash memory comprising:

a power source generating a reference voltage; and

an array wherein the array comprises a first plurality of transistors and a means for selecting, each of the first plurality of transistors coupled to the means for selecting, the array biased at the reference voltage and configured to provide a current for comparison with the flash memory.

2. The system of claim 1 wherein the reference voltage is internal, stable and independent from variations of a power supply or temperature

3. The system of claim 2 wherein each of the first plurality of transistors is in parallel.

4. The system of claim 3 further comprising a mirror transistor coupled to the array.

5. The system of claim 4 wherein a minimum voltage needed for the system is the threshold voltage of the mirror transistor plus the voltage across the array.

6. The system of claim 5 wherein the first plurality of transistors is rapidly switched on.

7. The system of claim 5 further comprising a plurality of sense amplifiers associated with the flash memory and a plurality of arrays, one of each of the plurality of sense amplifiers coupled to one of each of the plurality of arrays.

8. The system of claim 5 further comprising a plurality of sense amplifiers associated with the flash memory coupled to the array.

9. The system of claim 8 where the plurality of groups of transistors are N-channel transistors.

10. The system of claim 9 wherein the first plurality of transistors is configured such that at least one of the first plurality of transistors is activated with a signal in order to provide the current for comparison to the flash memory cell current.

11. The system of claim 10 further comprising a second plurality of transistors, one of each of the second plurality of transistors coupled to one each of

the first plurality of transistors, wherein the second plurality of transistors receive the signal and activate the first plurality of transistors.

12. The system of claim 11 wherein the reference voltage is modified in order to modify the current for comparison to the flash memory cell current.

13. A configurable mirror sense amplifier system for flash memory comprising:

a power source generating a reference voltage;

an array wherein the array comprises a plurality of transistors each of which is coupled to a means for selecting, the group of transistors biased at the reference voltage and configured to provide a current for comparison with the flash memory; and

a cascode structure coupled to the plurality of transistors and configured to bias the plurality of transistors in order to reduce Early effect.

14. The system of claim 13 further comprising a mirror transistor coupled to the cascode structure.

15. The system of claim 14 wherein the plurality of groups of transistors is configured such that at least one of the plurality of transistors is activated with a

signal, directed to the means for selecting, in order to provide the current for comparison to the flash memory cell current.

16. The system of claim 15 wherein the reference voltage is modified in order to modify the current for comparison to the flash memory cell current.

17. A method of configuring a mirror sense amplifier system for flash memory comprising:

determining a current sunk by one or more reference transistors;

selecting a configuration of at least one reference transistor based on the current sunk by the at least one reference transistor; and

comparing the sum of the current with a cell current of a memory cell in the flash memory.

18. A method of configuring a mirror sense amplifier system for flash memory comprising:

adjusting a gate voltage on a reference transistor such that the current flowing through the reference transistor is a suitable current reference; and

comparing the current with a cell current of a memory cell in the flash memory.

19. A method of configuring a mirror sense amplifier system for flash memory comprising:

selecting at least one transistor such that a sum of the current flowing through the at least one transistor approximates a suitable current reference;

adjusting the gate voltage on at least one of the at least one transistor such that the current flowing through the one or more groups of transistors approximates a suitable current reference; and

comparing the sum of the current with a cell current of a memory cell in the flash memory.